Physical Layout of High Current Rectifiers: Modern Methods for an Old Challenge

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Abstract— ***This paper address some problems linked to the physical layout of high current rectifier: paralleling components, magnetic field close to the rectifier and also the validation of the physical layout at reduced current. Even if the impact of cabling stray inductance is well known, some new tools and methodology are today available to design quicker and safer the physical layout of such high current rectifiers.***

I. Introduction

Electrochemical process of aluminium involves high DC currents, provided by high power rectifiers-transformer units (Fig.1.) [1]. If the global behaviour of these rectifiers is well known, the physical layout is still a challenging task for design engineers, since it impacts several issues simultaneously:

- Device design normally supposes a good current share between all SCRs of each secondary phase. However, this current division is affected by devices intrinsic property (but chips are often selected individually for high power structures) and also the layout of the rectifier itself. [1-4]
- Devices cooling must be accounted when choosing the rectifier layout
- The restrictions on magnetic close field in the aluminium plant are currently increasing, and also near the rectifier. This field map is obviously linked to the physical layout.

It is worth noting that the price and delays of such heavy realisations do not allow any trial and error method to design the rectifier layout.

In addition, for such high current converters, industry rarely provides test facilities, and the rectifier behaviour must be validated directly on the aluminium plant, what is always the most exciting point of the business… if all works well ! There is thus a strong need of internal validation, using smaller currents but allowing an extrapolation to nominal behaviour.

In this paper, it will be shown that the use of Computer Aided Design tools, associated with cabling rules, can help in proposing high current rectifier layouts, fulfilling all constraints. In addition, the comparison of simulation results to several tests at reduced current level will permit a first validation of the structure, and higher current extrapolation, before final test in the actual plant.

The paper will first investigate paralleling components issues, and especially remind the impact of transformer leakage inductance and layout parasitic. In addition, constraints on the matrix impedance representing the rectifier layout will be established. They may be useful to characterize and even optimize the layout (section II). Then, close field computation will be addressed (section III). In section IV, the example of a 40 kA booster will be proposed to illustrate the methodology.

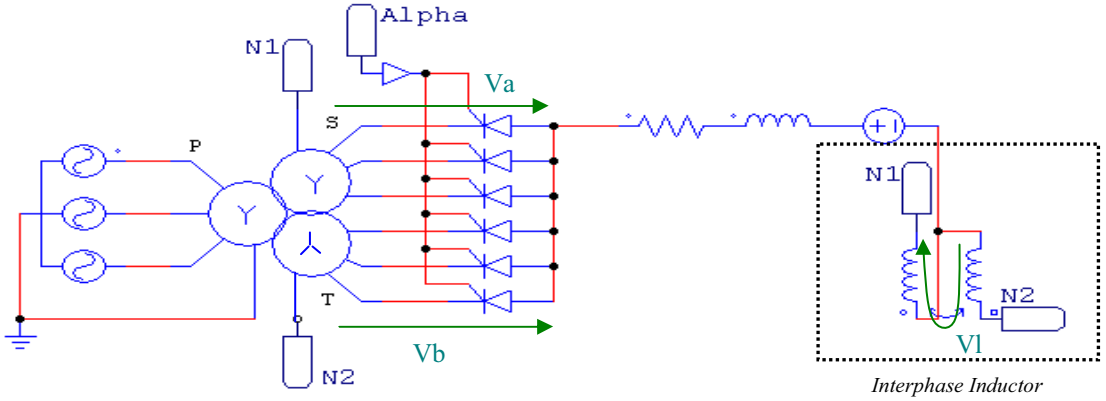

Fig. 1. Basic rectifier topology

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II. PARALLELING DEVICES ISSUES

The problem of paralleling several devices is well known and has been studied with the beginning of the rectifiers [1]. For high power, the components can be selected individually in order their characteristics match together. Therefore, potential dissymmetry is due to cabling only. Different impedance between the semiconductors, and also mutual couplings originate dynamic differences between all components [1-4]. Still today, even if all the reasons of current imbalance are (or at least should be) understood, the inverse problem is not easy to solve: how to find the right geometry to provide symmetrical electrical characteristics, even accounting for mutual coefficients ? Simulation can provide useful results to achieve this task. Indeed, even a geometrical symmetry does not guarantee symmetrical impedance matrix, when accounting for all mutual, as will be shown in section IV. Approximations proposed in [1] to simplify the computation may become wrong for modern rectifier with high integration ratio.

A first analysis of dynamical effects can be proposed, in order to investigate the problem of current division (Fig. 2.). During the commutation from one phase to the other, encroachment phenomenon occurs, mainly due to leakage inductance of the transformer. Global dI/dt of a phase is thus fixed, but the repartition between elementary components in each phase depends on the current divider formed by the cabling stray impedances. Stray impedance and mutual coupling must thus be accounted. It is worth noting from this simple model that all mutual inductance between all conductors have an impact, what is usually neglected in conventional design, where all phase legs are designed independently. The higher integration level may impose to account for all mutuals during the design, including the other phases.

Cabling rules, based on the same idea as [1], but without any assumption, have been proposed in [5] and can be adapted here, starting from the equivalent circuit of Fig. 2. To obtain synchronized turn on, all diode voltage of the same leg must be similar: this impacts on several mutual values and can be summarized with a simple cabling rule, which must be fulfilled thanks to the physical layout. Let's call K and L two phases of the rectifier. Phase K has n diodes, phase L m (usually m = n, but the formulation is general). At the end of the conduction of phase K, just before phase L being turned on, all diode voltage of phase L are expressed as a function of all currents and impedance parameters.

$$\begin{bmatrix} Vd1 \\ Vd2 \\ \vdots \\ Vdm \end{bmatrix}_L = \begin{bmatrix} \ddots & & \iddots \\ & M_{ij} & \\ \iddots & & \ddots \end{bmatrix} \cdot \frac{d}{dt} \begin{bmatrix} Iphase \\ Id1 \\ Id2 \\ \vdots \\ Idn \end{bmatrix}_K \quad (1)$$

$[M_{ij}]$ represents the mutual inductance matrix between the legs of phase L and all other conductors where current is flowing, including phase K. Iphase is the total current of phase K, and Id1…Idn each of the diode currents of phase K.

First, all voltage Vd1…Vdm must be equal. Second, assuming that the final layout will fulfil all conditions to have balanced currents, it can be supposed that Idi = Iphase/n. Therefore, (1) can be rewritten as:

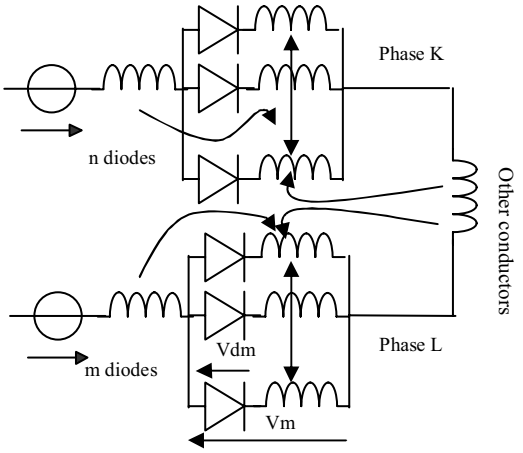


Fig. 2. Equivalent circuit during encroachment (all mutual are not displayed)

$$\begin{bmatrix} Vd \\ Vd \\ \vdots \\ Vd \end{bmatrix}_L = \begin{bmatrix} \ddots & & \iddots \\ & M_{ij} & \\ \iddots & & \ddots \end{bmatrix} \cdot \begin{bmatrix} 1 \\ 1/n \\ 1/n \\ \vdots \\ 1/n \end{bmatrix} \cdot \frac{dIphase}{dt}_K \quad (2)$$

(2) can be expressed as m cabling rules between mutual coefficients of the considered phase and the rest of the structure.

When all diodes are in the on state, obtaining the same currents necessitates fulfilling another set of rules, including both mutual inductance and stray impedance [5].

$$\begin{bmatrix} Vm \\ Vm \\ \vdots \\ Vm \end{bmatrix}_L = \begin{bmatrix} \ddots & & \iddots \\ & Z_{ij} & \\ \iddots & & \ddots \end{bmatrix} \cdot \frac{d}{dt} \begin{bmatrix} Iphase \\ Id1K \\ \vdots \\ IdnK \\ Id1L \\ \vdots \\ IdmL \end{bmatrix} \quad (3)$$

Voltage V1…Vm are leg voltages of phase m. All paralleled legs have the same voltage. Matrix $[Z_{ij}]$ links these voltage Vm to all currents of the structure: IdiK, currents of each leg of phase K, IdiL, currents of each leg of phase L, and Iphase, the global current. Assuming that the final layout will allow equal current division, leads to IdiK = Iphase/n and IdiL = Iphase/m. therefore, (3) can be expressed as:

$$\begin{bmatrix} Vm \\ Vm \\ \vdots \\ Vm \end{bmatrix}_L = \begin{bmatrix} \ddots & & \iddots \\ & Z_{ij} & \\ \iddots & & \ddots \end{bmatrix} \cdot \begin{bmatrix} 1 \\ 1/n \\ \vdots \\ 1/n \\ 1/m \\ \vdots \\ 1/m \end{bmatrix} \frac{dIphase}{dt} \quad (4)$$

As for (2), (4) corresponds to a set of m conditions on impedance matrix [Zij].
Even if these 2 sets of cabling rules cannot be used directly to find a proper layout for an inverter, they have been obtained without any assumption and therefore account for all couplings inside the system.
They can be used to qualify a tentative layout, or even in an optimization process to provide the "best" layout. Such procedures have been validated successfully in other applications [6].
Obtaining the complete impedance matrix of the system - necessary for the extraction of [Mij] and [Zij] - starting from the rectifier geometry is quite simple using Partial Element Equivalent Circuit method (PEEC) [7-8]. This modelling method allows attributing to each part of a circuit, a portion of the complete loop inductance. The complete geometry is thus decomposed into several massive segments, or bar. Analytical formula can be used to determine all inductance and mutual values, starting from the bar geometry only. To account for frequency effects, each bar can be meshed into elementary conductors. The final impedance matrix results from the association of all segments at desired frequency (Fig. 3).

III. Close Field Magnetic Radiated Emission

This issue becomes today more and more a challenge and must be accounted for new rectifiers. Indeed, due to high currents circulating in the system, magnetic field in the vicinity may be huge. Compensating loops are used for the complete plant, but they do not cancel the magnetic field around the rectifier itself. Therefore, people entering into the rectifier local may be exposed to magnetic fields exceeding the maximum allowed values for human health. Even if the effects are not well known, new standards begin to appear, and rectifier manufacturers are strongly encouraged to anticipate this new context. The same problem are encountered for instance when building railway substations [9].
Additionally, high magnetic field may disturb all surrounding electronics, especially the control boards of the SCRs, and all other control equipments. Therefore, the knowledge of the magnetic field will become a key point of rectifier design in the near future.

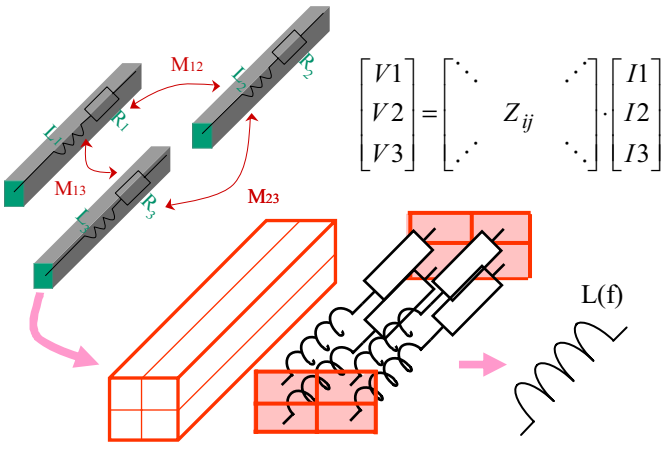


Fig.3. Illustration of PEEC Method.

The main cause of magnetic field shape close to the rectifier is due to cabling geometry. Finite elements method is not adapted for such large problems, time and memory consuming. Therefore PEEC method will be preferred. Obtaining magnetic induction close to the conductors is really simple using this approach: after modelling, the equivalent circuit is solved at desired frequency. Therefore, all currents in the elementary subdivisions are known. Then, Biot-Savard law can be easily used to compute magnetic field, since analytical formulation is available for an elementary bar [10]. The magnetic field in all free space around the rectifier is thus computed as the sum of all contributions of all elementary conductors.

IV. 40kAmps Booster Design

To illustrate how modelling can be useful in layout design, we propose here a complete study of a Booster, usually used in aluminium plant for helping the main rectifiers. In comparison with the main rectifier, the current rating of this booster is low, however, 40 kA is still a challenging design, regarding current division. 8 SCRs are used for each leg. Furthermore, since the testing facility is limited to 15 kA, the complete rectifier won't be actually tested before being installed in the actual plant, what lead the simulation especially interesting.

A. Rectifier structure

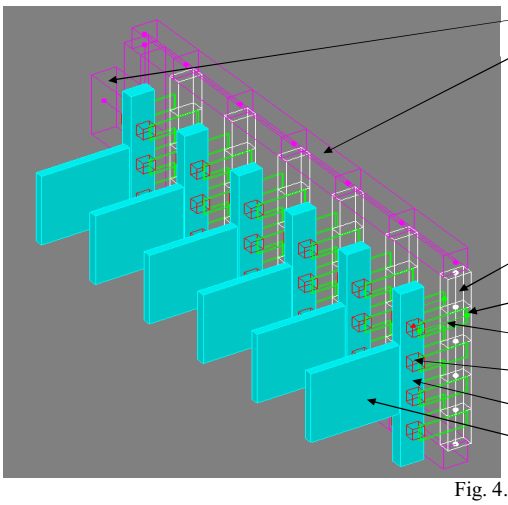
Fig.4. shows a layout proposal for rectifier implementation, as well as the electromagnetic modelling using PEEC method [11]. The basic structure is as symmetrical as possible, using a ladder structure (as proposed in [1]). Thermal management is achieved using a simple solution: the mechanical support for the SCR has also the electrical role of interconnection. Furthermore, hollow bars are used, allowing a liquid cooling.

B. Modelling and simulation

After modelling with PEEC method, an automatic circuit extraction system to a circuit simulator [12] allows obtaining all current waveforms in the components. Precise on-state characteristics have been taken into account, based on manufacturer datasheets. Von = 0.85 V, Ron = 89 μΩ.
Transformer is also important in the model, since leakage imposes the global current variation speed, as explained in the previous section. Since two secondary are needed, the equivalent circuit is not obvious. Complete equivalent circuits are available for multiwindings transformers [13], but they necessitate more data than usual datasheets.
Assuming the two secondary identical, we used the equivalent scheme of Fig. 5. Identifying all elements necessitates two short circuit voltage Ucc1 and Ucc2:

- Ucc1 to have nominal current when secondary 1 is short circuited,
- Ucc2 to have nominal current when both secondary are short circuited.

Unfortunately, only Ucc2 was given in the datasheet. We therefore used the empirical relation between L1 and L2: L1/L2 = R1/R2 = ¼, which has been validated for various transformers of such power.



(1) AC connections to the transformer,
(2) Bars, mechanical support for fuse
(3) Fuses
(4) Electrical link beteew SCR and Fuse
(5) Clamped SCR
(6) Bars, mechanical support for SCR,
(7) DC Bus conductors,
(8) DC connection to electrolyte
(9) DC breaker

Fig. 4. Physical layout proposal and associated modelling.

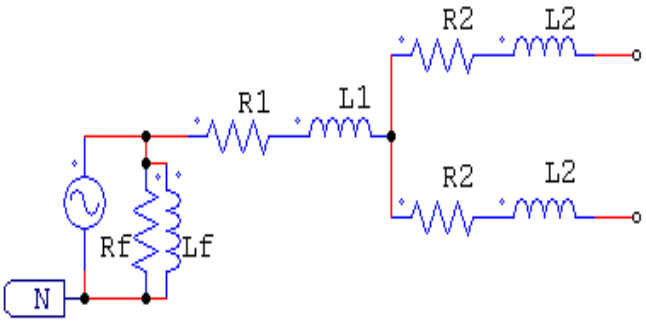


Fig. 5. Equivalent circuit used for one phase (all elements on the primary side)

The transformer had following characteristics:

2*2300 kVA
11000V – 165V
Ucc2 = 8%
Pcc2 = 76000 W

Based on Ucc2 and Pcc2, we obtained:
R1 = 0.14 Ω, L1 = 2.15mH
R2 = 0.56Ω, L2 = 8.6mH.

The temporal simulation results allow computing average and rms current mismatch, and current derating can be checked.
Fig. 6 illustrates the simulation results for phase 3, with the current division between the 8 SCRs, for nominal current. The geometrical implantation, as well as the SCR numbers are displayed on the top of this figure. The geometrical symmetry has obvious consequences, since SCR 1&4, 2&3, 5&8 and 6&7 have the same behaviour. However, it can be noticed that the coupling between phases is important, since SCRs 1&5 and 2&6 do not carry the same current.
These different temporal waveforms induce different mean and rms values, as illustrated in Table 1. The derating is computed with respect to the ideal case, where all SCRs would carry the same current. For a load current of 46545 A (corresponding to simulation conditions), the reference mean and rms currents can be easily computed, based on the normal behaviour of this structure (each secondary sees Idc/2 during a third of the period).

$$\text{Iavg/SCR} = \frac{46545}{2 \cdot 8} \cdot \frac{1}{3} = 970A$$

$$\text{Irms/SCR} = \frac{46545}{2 \cdot 8} \cdot \frac{1}{\sqrt{3}} = 1680A$$

The worst case of current division is for phase 2 and phase 1. This can be explained by their position in the rectifier and the impact of couplings with the rest of the structure. However, overall derating is below 30% what is reasonable. Indeed, the cooling system has been designed to account for a missing SCR in case of fault. With safety marging, this corresponds to a 40% derating.

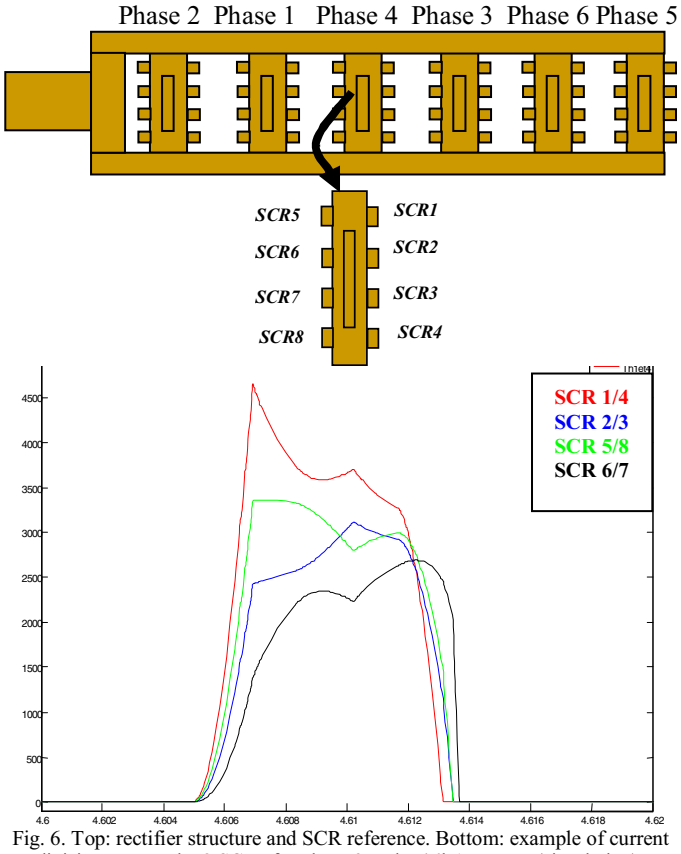


Fig. 6. Top: rectifier structure and SCR reference. Bottom: example of current division among the 8 SCRs for phase 3 and a 46kA current (simulation).

Table 1. Mean and Rms currents of all phases

Phase 1	SCR 1/4	SCR 2/3	SCR 5/8	SCR 6/7
Irms	2035	1540	1739	1351
Derating	21%	--	3.5%	--
Iavg	1194	917	1047	808.3
Derating	23%	--	8%	--
Phase 2				
Irms	2102	1588	1627	1163
Derating	25.1%	--	--	--
Iavg	1234	939	979	697
Derating	27%	--	0.9%	--
Phase 3				
Irms	1837	1434	1895	1510
Derating	9.34%	--	12.8%	--
Iavg	1083	877	1107	869
Derating	11.6%	--	14.1%	--
Phase 4				
Irms	1826	1328	1912	1401
Derating	8.7%	--	13.8%	--
Iavg	1083	812	1116	809
Derating	11.6%	--	15%	--
Phase 5				
Irms	1834	1550	1928	1423
Derating	9.2%	--	4.8%	--
Iavg	1077	863	1109	858
Derating	11%	--	14.3%	--
Phase 6				
Irms	1719	1353	1960	1447
Derating	2.3%	--	16.7%	--
Iavg	1014	766	1141	874
Derating	4.5%	--	17.6%	--

Another way of investigating the quality of the proposed layout is to check the cabling rules presented section II. This is all the more interesting that it avoids the heavy process of modifying the geometry, then running a long temporal simulation, analyzing the results and modifying the geometry again… Proposed cabling rules keep the link between geometry and electrical characteristics, and therefore are suitable to build an optimization process: the geometry will be modified according to the cabling rules criteria, using an appropriate optimization algorithm. This solution has been carried out successfully in another application [6]. In this case however, this has not been necessary since the SCR derating was considered acceptable.

C. Experimental validation

Several "low current" (10 kA and 15 kA) validations have been carried out, to check the validity of the simulation (example Fig. 7 and Fig. 8), and to validate cooling aspects. At 10 kA, only 2 SCRs per phase were kept, to validate the cooling.

The "low power" transformer was identified, since it was obviously different from the one designed for the 40 kA rectifier, and a new set of temporal simulations was carried out.

Fig. 7. shows the very good agreement between measured current in SCR #6 of phase 1. Experimental conditions were Idc = 10kA, obtained in short circuit with a firing angle of 71°, and only 2 SCRs (5&6). Other measurements with SCRs 1&2 have also given the same good results. Fig. 8. illustrates the superposition of simulated and measured currents in SCR 1&2 of phase 1 in the same operating conditions. In this case, the current division is not as bad as in the simulation of Fig. 6, since operating conditions are different: the transformer is not the same, current level is lower, and all SCRs are not used.

Some experimental results were also achieved at 15k A with all SCRs, but all currents could not be recorded, due to the number of current probe and space needed. The measurement of voltage drop across the fuses in series with the SCR allows a rough estimate of the current flowing through the device. This has confirmed the tendency obtained in the simulation: the most loaded devices are the external ones (1&4 and 5&8)

In conclusion, the good agreement between current commutation speed in one SCR validates the PEEC model of the rectifier, because it is only due to cabling impedance. Furthermore, the tendency when using all 8 SCRs has also been validated.

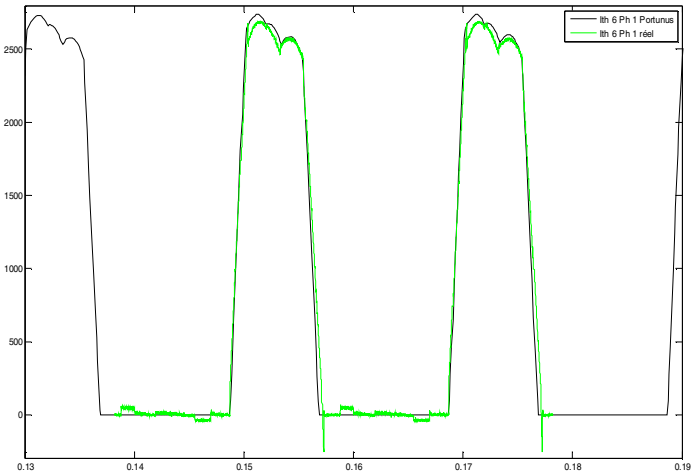


Fig.7. Comparison of simulated and experimental results for SCR #6 phase 1 in the case of a 10kA test with 2 SCRs

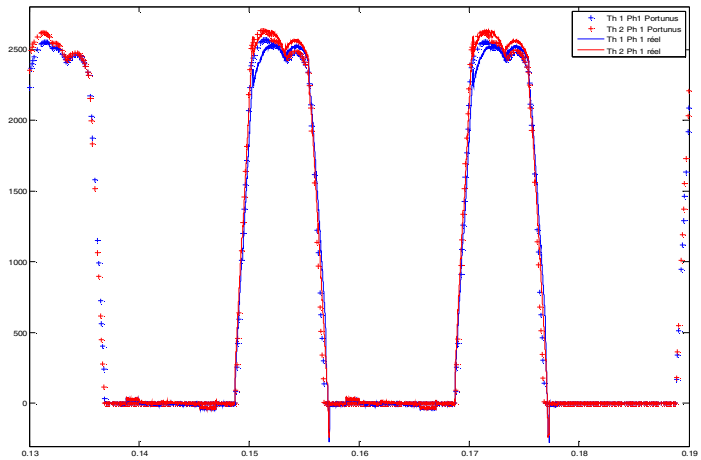


Fig.8. Comparison of simulated and experimental results for SCR #1&2 phase 1 in the case of a 10kA test with 2 SCRs.
Solid lines: simulation. Cross: measurement

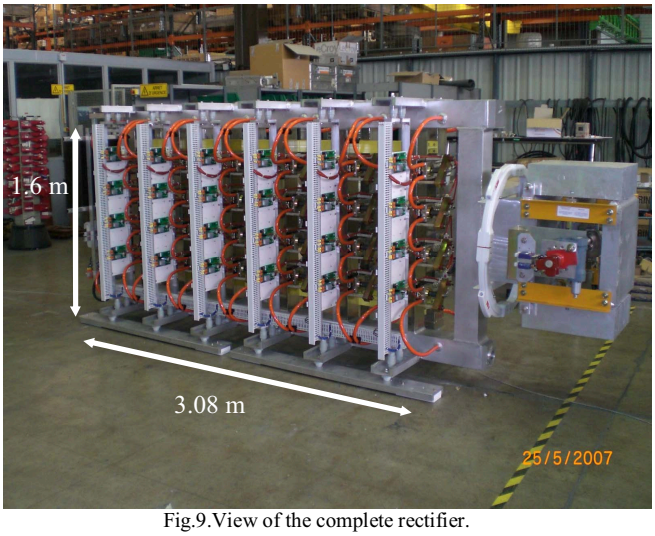


Fig.9.View of the complete rectifier.

D. *Close field map*

After the converter modelling validation, we focused on near magnetic field. The field spectrum obviously contains a DC part but also AC components, due to the waveforms of the SCR currents. By using Fourier series, the AC magnetic field can be obtained by superposition of several field maps at various frequencies, representing the harmonic decomposition of SCR currents. Due to the decrease of harmonic amplitude with they order, we only focused on the fundamental component (50Hz). To be noted that the DC field is much more restrictive for all the control boards of the SCRs and the electrical cabinets.

Positioning of the cartography grids.

Magnetic induction will be computed and plotted on a grid, defined Fig.10. Three different distances were defined in order to investigate the decrease of the field with the distance (0.5m, 1m and 1.5m). The high of the gird has been chosen 3 m higher than a human.

Some results are given on Fig. 11. for DC component and Fig.12 for 50Hz AC field. It is worth noting that the induction global shape is more complex near the rectifier than far from it.

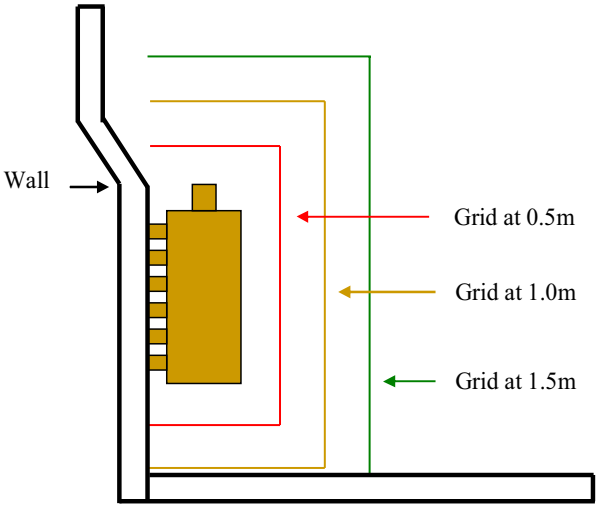


Fig.10. Grid definition for magnetic field computation

This can be explained by the multipole expansion theory [14]: far from a radiating source, only the dipole term is preponderant, whereas near the device, higher orders appear.

Compared to DC, induction shape is changed at 50Hz, as illustrated Fig.12. This is due to the different localization of AC currents, compared to DC currents.

All results are summarized in Table 2. Induction stays at low values at any distance and frequency, what is reassuring for human exposure (service engineering). Furthermore, control boards of SCR have been tested at 150 Gauss DC fields without any problem.

Table 2. Summary of max and minimum induction values.

		0.5 m	*1.0 m*	*1.5 m*
DC Field	Maximum Value (Gauss)	*50*	*30*	*20*
	Minimum Value (Gauss)	*0.309*	*0.076*	*0.0141*
AC Field	Maximum Value (Gauss)	*10*	*2.7*	*1.3*
	Minimum Value (Gauss)	*0.21*	*0.31*	*0.166*

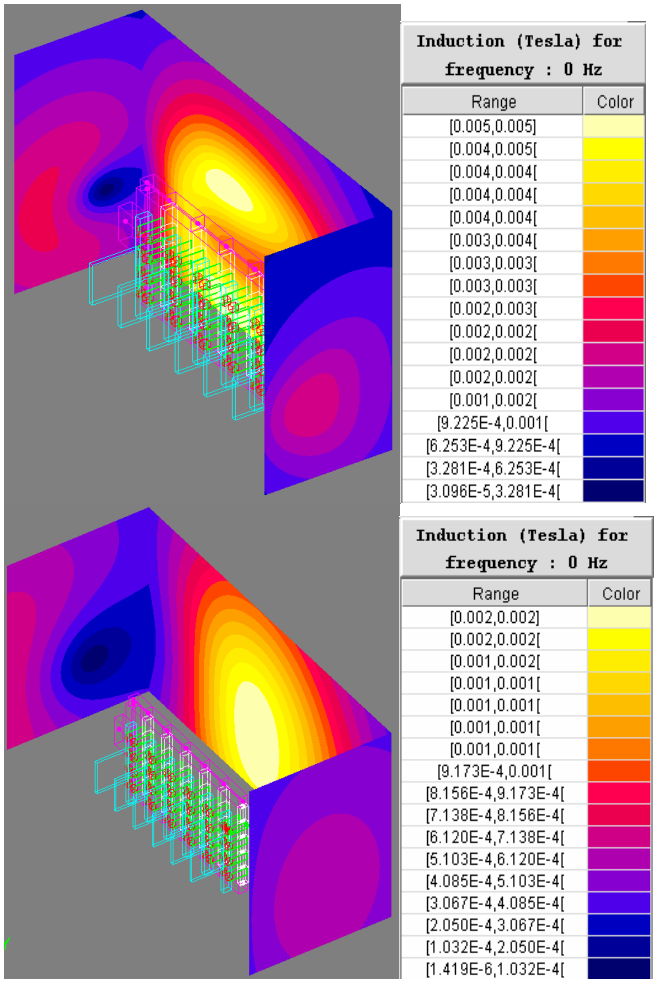


Fig.11. DC Induction at 0.5m (top and 1.5m (Bottom)

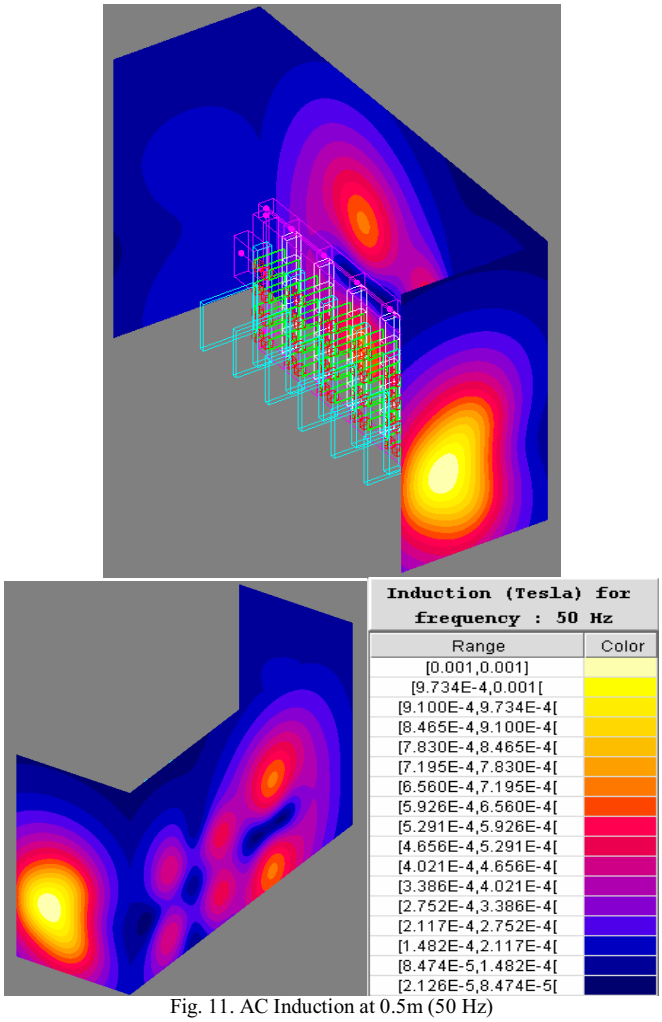


Fig. 11. AC Induction at 0.5m (50 Hz)

V. CONCLUSION

High current rectifier layout impacts on several aspects and mainly current division, as well as induction radiated around the converter. Even if the problem of current division is known since tens of years, new modelling tools allow a better precision for layout investigation. PEEC method is well adapted for this purpose. It provides an electrical equivalent circuit of the converter layout. A coupling with simulation software allows a direct analysis of temporal current waveforms. Cabling rules have also been presented: starting from the equivalent modelling of the converter, they give restrictions on impedance matrix of the system, in order to guarantee a good current division. The use of these rules allows avoiding temporal simulation, and opens the possibility of automatic layout optimization of such high power rectifiers.

Another aspect can be handled with PEEC method: magnetic induction around the converter can be computed, and compared to existing or future standards.

All these issues are now easy to be addressed before actual design, thank to simulation software. This will allow many saves in such high power engineering design activities.

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